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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,384	03/05/2002	Jin-Gyeong Kim	INTV.008A	8452

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ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

EXAMINER	
VO, TUNG T	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/092,384	KIM ET AL.	
	Examiner	Art Unit	
	Tung Vo	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuji et al. (US 5,898,695) in view of Aoki et al. (US 5,771,331).

Re claims 1-3 and 5-7, Fuji teaches a data buffer circuit (203 of fig. 17) for a video decoder (fig. 17) comprising: a receiver circuit (200 of fig. 17) adapted to receive a video bitstrenm; a ring buffer (203 of fig. 17, e.g. RAM (203) is packet landing buffer that is described in figure 6 is a ring buffer) adapted to store the video bitstream; and an error resilience module (205 of fig. 17, e.g. micro-processor is adapted to select and send video data from the ring buffer (203 of fig. 17), wherein the demodulator (2 of fig. 17) demodulates the channel data which was channel encoded by QAM, QPSK, or the like, performs an error correction process by using redundancy codes, and supplies the processed data to a demultiplexer (3 of fig. 17) to the decoder (207 of fig. 17), see also fig. 21) adapted to retrieve data from the ring buffer, wherein the . Re claim 2, Fuji further discloses wherein the receiver circuit (200 of fig. 17) comprises a wireless receiver (1 of fig. 16, e.g. a communications satellite); a log interface circuit (215 of fig. 17, e.g. error flag delay or buffer adapted to store the data logging information, col. 12, lines 12, lines 33-39, the error flag is added to the encoded bitstream to indicate whether or not an error in

the encoded bistream), adapted to store data logging information in the ring buffer such that the data logging information is aligned with corresponding data from the video bitstream, a data buffer circuit for a video decoder (figure 17) comprising: means (200 of fig. 17) for receiving a video bitstream; means (201 of fig. 17) for inspecting the video bitstream for error; means (203 of fig. 17) for storing the video bitstream in a ring buffer regardless of an error indication; means (215, 217 of fig. 18, e.g. the error flag is added into encoded bitstream, wherein the error flag and encoded bitstream stored in the RAM (203 of fig. 17) instructed by the micro- processor (204)) for storing data logging information corresponding to video bitstream data in the ring buffer in an aligned manner with the corresponding video bitstream data; and means (204 of fig. 17, e.g. select and send video data to the video decoder 207 of fig. 17 based on the user input (13 of fig. 16)) for automatically retrieving both a portion of the video bitstream and a corresponding portion of the data logging information from the ring buffer in response to a request for data.

Moreover, Fuji further teaches wirelessly receiving the video bitstream (1 of fig. 16) and an error resilience module (201 of fig. 17) operable to select (detecting the input signal from demodulator 200 of fig. 17, error or no error occurs), the selection responsive to analysis of the video bitstream in both a forward direction and a reserve direction as accessed via the ring buffer (B represents Bidirectional frame or picture as considered forward and reserve directions, of the video bistream, see col. 7, lines 50-65).

It is noted that Fuji does not particularly teach the ring buffer allows data to be access "by both sequentially increasing memory address and sequentially decreasing memory addresses", "storing the video bitstream in a ring buffer subsequently to the video bitstream being inspected

for error and prior to correction thereof", and mean for storing data logging information corresponding to the video bitstream in the ring buffer" as claimed.

However, Aoki teaches a ring buffer (4 of fig. 1) allows data to be access by both sequentially increasing memory address and sequentially decreasing memory addresses (fig. 4b, e.g. FIG. 4b shows a state in which the read pointer RP advances to an address position R2 to read data out of the ring buffer 4, decreasing the unread data area and increasing the already-read data area) , storing the video bitstream in a ring buffer subsequently to the video bitstream being inspected for error and prior to correction thereof (3 and 4 of fig. 1, e.g. sector detection circuit is detecting the video bitstream and transmits the video bitstream into the ring buffer 4 of fig. 1), and mean (8, 8-2 of fig. 1, e.g. RP stored in the ring buffer 4) for storing data logging information corresponding to the video bitstream in the ring buffer.

Taking the teachings of Fuji and Aoki as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the ring buffer (fig. 1) of Aoki into the buffer circuit of Fuji to produce a double-speed and increase the capacity of buffer during the video bistream being decoded. Doing so would allow the video decoder to correct the error while decoding video bitstream.

3. Claims 4 and 8-10 rejected under 35 U.S.C. 103(a) as being unpatentable over Fuji et al. (US 5,898,695) in view of Aoki et al. (US 5,771,331) as applied to claims 1 and 6, and further in view of Kadono (US 6,757,332 B1).

Re claims 4, 8-10, Fuji further teaches the decoder for receiving the video bitstream in an MPEG compliant decoder (207 of fig. 17, see col. 1 for MPEG specification of Fuji); decoding

the video bitstream (202 of fig. 17, e.g. decoding before storing the video bitstream in the ring buffer) prior to storing the video bitstream in the ring buffer, and wherein the storing of the video bitstream comprises storing the decoded form (73 of fig. 16, e.g. system decode buffer for storing the decoded bitstream, wherein the system decode buffer is a part of the RAM (7 of fig. 16, and packet landing buffer (71 of fig. 16, 203 of fig. 17) is also a part of the RAM, therefore the R.AM capable of storing the decoded bitstream); decoding the video bitstrenm after the video bitstream has been stored in the ring buffer (203, 204, and 207 of fig. 17, e.g. the video decoder (207 of fig. 17) decodes the video bitstream is read from the ring buffer (203) by the micro-processor (204) to produce a decoded bitstream).

It is noted that Fuji and Aoki teach the MPEG decoder but not a MPEG-4 decoder for decoding video object planes in the video stream as claimed.

However, Kadono teaches an MPEG-4 compliant decoder (102 of fig. 1 and fig. 5, see also col. 2) for encoding a VOP of the video stream (VOP stream) based on the error notification (304 of fig. 5).

Therefore, taking the teachings of Fuji, Aoki and Kadono as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the MPEG-4 compliant decoder of Kadono into the video bitstream decoder (fig. 17) of Fuji and Aoki for the same purpose of decoding any video encoded bitstreams.

Doing so would provide degradation in picture quality due to presence of encoded of un-received picture is avoided, and the operation of a buffer memory is prevented from being impeded by unnecessary encoded data.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung Vo whose telephone number is 571-272-7340. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris. Kelley can be reached on 571-272-7331. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tung Vo
Primary Examiner
Art Unit 2613